ABSTRACT

An electrically addressable data storage unit has a matrix of rows and columns of data storage arrays on a single substrate. Each array is a matrix of coplanar data storage diode cells connected by row lines and column lines for recording, addressing and reading of data. The address lines and power lines of the plurality of arrays are connected to the arrays so that only the data storage diode cells in the array of a selected data storage cell are enabled, thereby eliminating undesirable power dissipation in all other arrays of the data storage unit.

A plurality of row address lines are each in contact through row decoders with the rows of all of the arrays in one of the columns of the data storage arrays. A plurality of column address lines are each in contact through column decoders with the columns of all of the arrays in one of the rows of the data storage arrays. A controller enables the row and column address lines to selectively address a data storage diode cell in a selected array.

A plurality of row power lines are each connected to the rows of one array in the multiple arrays, and a plurality of column power lines are each connected to the columns of one array in the multiple arrays. The row and column power lines connected to the selected array are provided with values to enable the selected data storage diode cell. The row and column power lines connected to all arrays other than the selected array are provided with values to disable the data storage diode cells of the other arrays, thereby eliminating undesirable power dissipation from the other arrays.